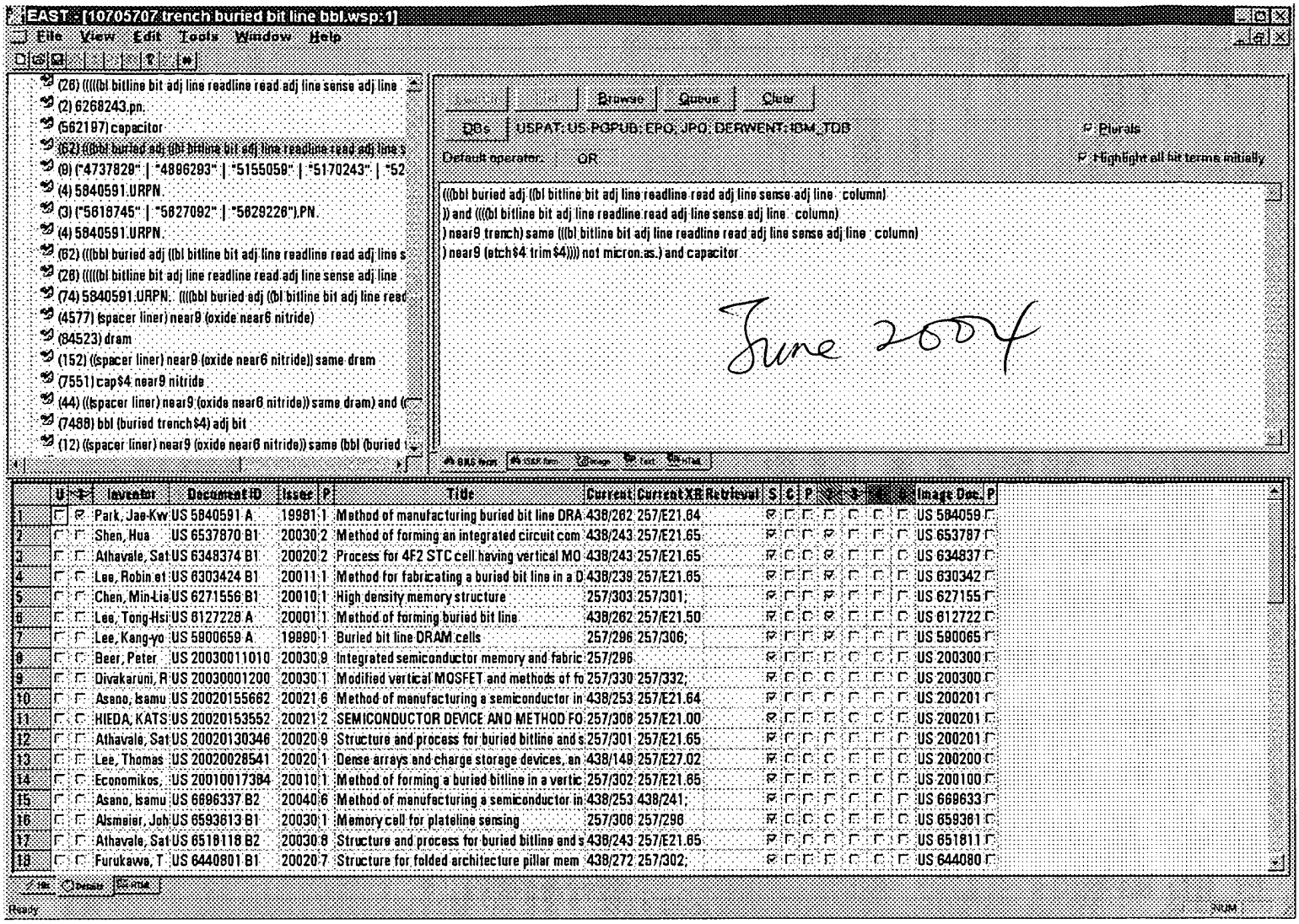

	U	↕	Inventor	Document ID	Issue	P	Title	Current	Current XR	Retrieval	S	C	P	↕	↕	↕	↕	Image Doc.	P
1	☐	☑	Park, Jae-Kw	US 5840591 A	19981	1	Method of manufacturing buried bit line DRA	438/262	257/E21.64		☑	☐	☐	☐	☐	☐	☐	US 584059	☐
2	☐	☐	Shen, Hua	US 6537870 B1	20030	2	Method of forming an integrated circuit com	438/243	257/E21.65		☑	☐	☐	☑	☐	☐	☐	US 653787	☐
3	☐	☐	Athavale, Sat	US 6348374 B1	20020	2	Process for 4F2 STC cell having vertical MO	438/243	257/E21.65		☑	☐	☐	☑	☐	☐	☐	US 634837	☐
4	☐	☐	Lee, Robin et	US 6303424 B1	20011	1	Method for fabricating a buried bit line in a D	438/239	257/E21.65		☑	☐	☐	☑	☐	☐	☐	US 630342	☐
5	☐	☐	Chen, Min-Lia	US 6271556 B1	20010	1	High density memory structure	257/303	257/301;		☑	☐	☐	☑	☐	☐	☐	US 627155	☐
6	☐	☐	Lee, Tong-Hsi	US 6127228 A	20001	1	Method of forming buried bit line	438/262	257/E21.50		☑	☐	☐	☑	☐	☐	☐	US 612722	☐
7	☐	☐	Lee, Kang-yo	US 5800659 A	19980	1	Buried bit line DRAM cells	257/296	257/306;		☑	☐	☐	☑	☐	☐	☐	US 580065	☐
8	☐	☐	Beer, Peter	US 20030011010	20030	9	Integrated semiconductor memory and fabric	257/296			☑	☐	☐	☐	☐	☐	☐	US 200300	☐
9	☐	☐	Divakaruni, R	US 20030001200	20030	1	Modified vertical MOSFET and methods of fo	257/330	257/332;		☑	☐	☐	☐	☐	☐	☐	US 200300	☐
10	☐	☐	Asano, Isamu	US 20020155662	20021	6	Method of manufacturing a semiconductor in	438/253	257/E21.64		☑	☐	☐	☐	☐	☐	☐	US 200201	☐
11	☐	☐	HIEDA, KATS	US 20020153552	20021	2	SEMICONDUCTOR DEVICE AND METHOD FO	257/308	257/E21.00		☑	☐	☐	☐	☐	☐	☐	US 200201	☐
12	☐	☐	Athavale, Sat	US 20020130346	20020	9	Structure and process for buried bitline and s	257/301	257/E21.65		☑	☐	☐	☐	☐	☐	☐	US 200201	☐
13	☐	☐	Lee, Thomas	US 20020028541	20020	1	Dense arrays and charge storage devices, an	438/149	257/E27.02		☑	☐	☐	☐	☐	☐	☐	US 200200	☐
14	☐	☐	Economikos,	US 20010017384	20010	1	Method of forming a buried bitline in a vertic	257/302	257/E21.65		☑	☐	☐	☐	☐	☐	☐	US 200100	☐
15	☐	☐	Asano, Isamu	US 6696337 B2	20040	6	Method of manufacturing a semiconductor in	438/253	438/241;		☑	☐	☐	☐	☐	☐	☐	US 669633	☐
16	☐	☐	Alsmeier, Joh	US 6593613 B1	20030	1	Memory cell for plateline sensing	257/308	257/298		☑	☐	☐	☐	☐	☐	☐	US 659361	☐
17	☐	☐	Athavale, Sat	US 6518118 B2	20030	8	Structure and process for buried bitline and s	438/243	257/E21.65		☑	☐	☐	☐	☐	☐	☐	US 651811	☐
18	☐	☐	Furukawa, T	US 6440801 B1	20020	7	Structure for folded architecture pillar mem	438/272	257/302;		☑	☐	☐	☐	☐	☐	☐	US 644080	☐